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I2S Bus Transceiver

Features

I2S Compliance

- ✓ Comply with I2S Bus Spec from Philips Semiconductor
- ✓ Flexible configuration for sample rate and bit width
- ✓ Silicon Proven

FPGA / ASIC Integration

- ✓ RTL code in System Verilog
- ✓ Elastic Buffer built-in for clock domain crossing
- ✓ No external FIFO needed
- ✓ Modelsim simulation library provided for free download
- ✓ Easy to use, Easy to integrate

Applications

- ✓ VoIP (Voice over IP)
- ✓ Digital Walkie-Talkie
- ✓ Speech Recording

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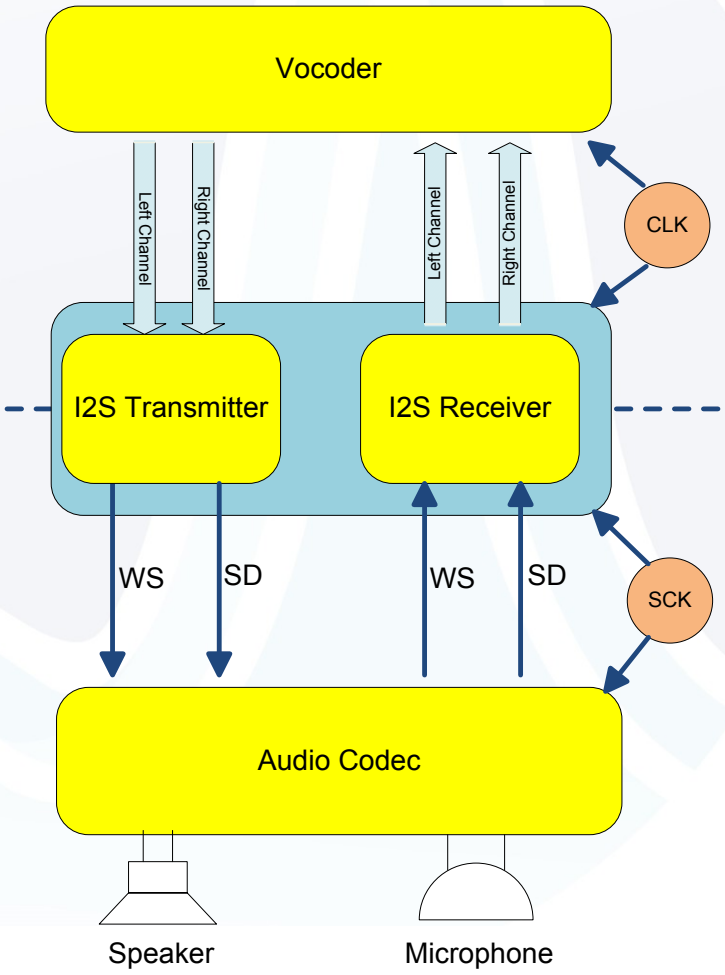
Introduction

I2S is a popular bus protocol used by audio codec ICs to transfer PCM samples. PulseRain Technology's silicon proven I2S transceiver offers a seamless solution for audio codec / vocoder integration. It can be configured flexibly for various sample rate and bit width. Due to its smart elastic buffer design, CDC (Clock Domain Crossing) and flow control are turned into cinches during IP integration.

Block Diagram



IP Implementation and Quality Metrics

Clock Rate (CLK)	*80 MHZ*
Clock Rate (SCK)	*12 MHZ*
Sample Rate	*8 KHZ*
Word Length (Bit Width)	*16 bit*
FPGA Device	*Altera EP3C120F780C7*
Synthesis	*Quartus 13.1 64-bit version*
Place and Route	*Quartus 13.1 64-bit version*
Total Logic Elements	*527 / 119,088 (< 1%)*
Total Comb functions	*280 / 119,088 (< 1%)*
Dedicated logic registers	*492 / 119,088 (< 1%)*
Total Registers	*492*
Total Memory Bits	*0 / 3,981,312 (0%)*
Embedded Multiplier (9 bit)	*0 / 576 (0%)*

Device Implementation Matrix - **Altera Cyclone III Family**

Verification

- ✓ Gone through extensive simulations with various combination of bit width, sample rate and clock rate.
- ✓ Pass extensive Synthesis, Place and Route iterations.
- ✓ Silicon Proven on Altera Cyclone III Development Kit, plus a daughter card from Terasic for audio codec.

Deliverable

This IP core is available in the form of:

- RTL source code (System Verilog)
- or, in obfuscated source code
- or, in FPGA device netlist

And the release package will include:

- the IP core in certain form
- Release notes
- ICD (Interface Control Document)
- Modelsim simulation library
- Testbench
- Scripts for simulation or synthesis