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G723.1 Dual Rate Decoder

Features

G723.1 Compliance

- ✓ G723.1 dual rate decoder (5.3 kbps and 6.3 kbps)
- ✓ Support G723.1 Annex A
- ✓ Support multi-channel input
- ✓ Pass all test vectors provided by ITU
- ✓ Silicon Proven

FPGA / ASIC Integration

- ✓ RTL code in System Verilog
- ✓ No DSP core needed
- ✓ No co-processor needed
- ✓ Industry's highest data throughput per clock cycle
- ✓ Modelsim simulation library provided for free download
- ✓ Easy to use, Easy to integrate

Applications

- ✓ VoIP (Voice over IP)
- ✓ Digital Walkie-Talkie
- ✓ Speech Recording

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ITU G723.1 is a widely used vocoder standard for Voice over IP. It is able to offer very low bit rate (as low as 5.3kbps) with high voice quality, which makes it stand out amongst its peers.

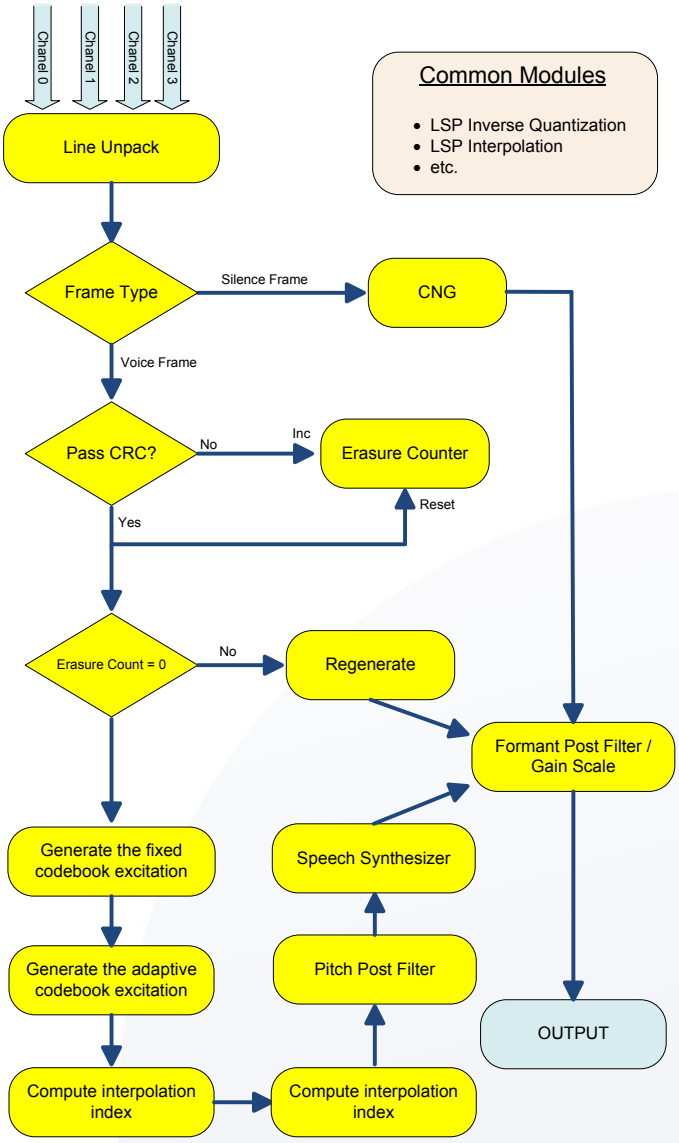
On top of that, the G723.1 Annex A supports VAD (Voice Activity Detection) and CNG (Comfort Noise Generation). Such features find their ways not only in bandwidth reduction for VoIP applications, they can also be used as VOX (Voice Operated eXchange) switch for walkie talkies, especially for those ones operating in digital mode.

Having said that, the G723.1 is also known for being computation-intensive, thanks to many of the elaborate algorithms it incorporates and the convoluted control flows that come with them. Consequently, all implementation schemes offered on the market today demand the availability of DSP cores with high MIPS capability. And multi-channel implementation is largely done by consuming more MIPS or increasing the number of DSP cores.

Fortunately, PulseRain Technology has broken the status quo by introducing the world's first FPGA / ASIC based multi-channel G723.1 codec. As for the decoder part, it supports both 5.3 kbps low rate and 6.3 kbps high rate decompression, with Annex A included. It features the industry's highest data throughput per clock cycle. And the typical configuration runs at 80MHZ clock rate with input of 4 channels.

The decoder has gone through rigorous verification process in both simulation and silicon. It has passed the full set of ITU test vectors with input of 4 channels. It is also silicon proven on an Altera cyclone III FPGA Dev Kit. Random packet loss has been emulated by hardware to verify the PLC (Packet Loss Concealment) capability of G723.1.

Block Diagram



The above diagram shows the major function blocks inside the decoder. Each input represents a frame received on respective channels. To conform to the G723.1 standard, the post filters can be bypassed through pin configuration. And the frame will be regenerated based on past data when erasure is detected.

IP Implementation and Quality Metrics

Num of Channels	*4*
Clock Rate	*80 MHZ*
FPGA Device	*Altera EP3C120F780C7*
Synthesis	*Quartus 13.1 64-bit version*
Place and Route	*Quartus 13.1 64-bit version*
Total Logic Elements	*17,353 / 119,088 (15%)*
Total Comb functions	*15,028 / 119,088 (13%)*
Dedicated logic registers	*10,738 / 119,088 (9%)*
Total Registers	*10738*
Total Memory Bits	*187,079 / 3,981,312 (5%)*
Embedded Multiplier (9 bit)	*78 / 576 (14%)*

Device Implementation Matrix - **Altera Cyclone III Family**

Verification

- ✓ Pass All test vectors provided by ITU, with input of 4 channels.
- ✓ Pass extensive Synthesis, Place and Route iterations.
- ✓ Silicon Proven on Altera Cyclone III Development Kit, plus a daughter card from Terasic for audio codec.
- ✓ Packet loss has been emulated by hardware to confirm the Packet Loss Concealment capability of G723.1

Deliverable

This IP core is available in the form of:

- RTL source code (System Verilog)
- or, in obfuscated source code
- or, in FPGA device netlist

And the release package will include:

- the IP core in certain form
- Release notes
- ICD (Interface Control Document)
- Modelsim simulation library
- Testbench
- Test Vectors
- Scripts for simulation or synthesis